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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,996	10/30/2003	Mark Own Homewood	S1022.81044US00	7394

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,996	HOMEWOOD ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Europe on November 2002. It is noted, however, that applicant has not filed a certified copy of the 02257603.7 application as required by 35 U.S.C. 119(b).

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the examiner notes its is a copy of claim 1 of the application and further contains legal phraseology “said data” in line 7 page 15. Correction is required. See MPEP § 608.01(b).

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The disclosure is objected to because of the following informalities:

"10 000" of page 6 line 2.

The applicant is required to review the entire specification and correct all grammatical and typographical errors.

Claim Objections

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 23 recites dependency on claim 23, page 13.

Claim Rejections - 35 USC § 112

7. Claims 13 and 25 recite the limitation "said different signal" in line 29 of claim 13 on page 11 and line 24 of claim 25 on page 13. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 is dependent on claim 5 whereas "different signal" is introduced in claim 10 lines 14 and 15 of page 11.

Claim 25 is dependent on 24 there is no mention of a "different signal" in claims 24 and 25 prior to line 24 on page 14.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1 - 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Baker et al (U.S. Patent No. 6,434,649 henceforth Baker).

10. As to Claim 1, Baker teaches a system comprising:

a processor for executing instructions; (column 1, lines 24 – 36)

a stream register unit connected to supply data from the peripheral to the processor (column 1, lines 24 – 36);

a FIFO connected to receive data from the peripheral and connected to the stream register unit by a communication path, along which the said data can be supplied from the FIFO to the stream register unit; and (column 7, lines 6 – 11)

a memory bus connected between the data memory and the processor, across which the processor can access the randomly accessible data (column 1, lines 24 – 36).

The examiner interprets a stream register, as being equivalent to the data bus master in Baker and hereinafter will follow for claims 1 thru 30.

11. As to claim 2, Baker teaches a system, wherein the stream register unit forms part of the processor (column 5, lines 52 – 67).

12. As to claim 3, Baker teaches a system, wherein data is supplied from the FIFO to the stream register unit accordance with requests for data made by the processor to the stream register unit and forwarded to the FIFO (column 7, lines 6 –22).

13. As to claim 4, Baker teaches a system, wherein the said requests are made as accesses to volatile variables (column 26 lines 1 – 36).

14. As to claim 5, Baker teaches a system wherein the FIFO is arranged to, upon receiving a request for data from the stream register unit, send a signal to the stream register unit indication availability of the requested data (column 12, lines 37 –43).

15. As to claim 6, Baker teaches a system, wherein if the FIFO contains the requested data, the said signal to the stream register unit indicates that the data is available, and the FIFO is further arranged to send a signal to the stream register unit comprising the data (column 12, lines 35 – 46).

16. As to claim 7, Baker teaches a system, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, supply the data to the processor (column 12, lines 56 – 62).

17. As to claim 8, Baker teaches a system, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, send a signal to the FIFO indicating that it has taken the data (column 13, lines 1 – 15).

18. As to claim 9, Baker teaches a system, wherein the said signal to the FIFO further indicates the next location in the FIFO from which the data is required (column 13, lines 41 – 49).

19. As to claim 10, Baker teaches a system, wherein the FIFO is further arranged to, if it does not contain the requested data, send a different signal to the stream register unit indicating that the data is not available (column 24, lines 54 - 67).

20. As to claim 11, Baker teaches a system, wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions (column 24, lines 54 - 67).

21. As to claim 12, Baker teaches a system, wherein the FIFO is further arranged to, if following sending of the said different signal to the stream register unit indicating that the data is available and to send a signal comprising the data to the stream register unit (column 24, lines 54 - 67).

22. As to claim 13, Baker teaches a system, further comprising a timeout generator, arranged for communication with the processor and the stream register unit, and arranged to, if the signal sent by the FIFO is a different signal indicating that the data is not available, after a predetermined period of time, send a timeout signal to the processor, causing the processor to interrupt such that it can execute other instructions (column 24, lines 21 – 53).

23. As to claim 14, Baker teaches a system, wherein if following sending of the timeout signal to the processor the data subsequently becomes available, the timeout generator is arranged to receive a signal instructing it to cease sending the timeout signal, and to, upon receipt of the said instruction, cease sending the timeout signal (column 24, lines 21 – 53).

The examiner makes a note to point out an interpretation in the difference between a timeout and a stall. A timeout is used to interrupt a process that has been waiting for an expected event where as stall puts a halt on the processor until recovered. Baker teaches a system containing 64 individual buffer FIFOs (column 19, lines 10 – 15) and both stall and timeout are adequately described by Baker relevant to the application.

24. As to claim 15, Baker teaches a system, wherein the stream register unit is associated with a register file containing a plurality of registers and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file (column, lines).

25. As to claim 16, Baker teaches a system, wherein the stream register unit is associated with a register file containing a plurality of registers and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file (column 18, lines 13 – 67, column 19, lines 1 - 67).

26. As to claim 17, Baker teaches a system, wherein the processor is arranged to retrieve data from the register file (column 19, lines 1 - 67).

27. As to claim 18, Baker teaches a system, wherein data is supplied form the FIFO to the stream register unit in accordance with requests for data made by the processor to the stream register unit and forwarded to the FIFO, wherein the stream register unit is associated with a register file containing a plurality of registers and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file, wherein the processor is further arranged to make requests for data to the stream register unit via the load/store unit (column 18, lines 13 – 67, column 19, lines 1 - 67).

28. As to claim 19, Baker teaches a system, wherein the stream register unit comprises one or more FIFOs connected to receive data from the FIFO connected to the stream register and supply the data to the processor (column 19, lines 11 – 14).

29. As to claim 20, Baker teaches a system, wherein the request for data is a request for a single data item (column 21, lines 44 – 67).

30. As to claim 21, Baker teaches a system, further comprising one or more additional FIFOs linked together between the said FIFO and the communication channel (figure 9, column 29, lines 33 – 63).

31. As to claim 22, Baker teaches a system, wherein the data from the peripheral is video data (column 8, lines 29 – 58).

32. As to claim 23, Baker teaches a system, wherein the peripheral is a video processing system (column 8, lines 29 – 58).

33. As to claim 24, Baker teaches a system, comprising:

a processor (column 1, lines 24 – 36);

a stream register associated with the processor (column 1, lines 24 – 36);

a FIFO memory connected to the processor via the stream register (column 7, lines 6 – 11),

wherein the stream register and the FIFO operate the same data handling protocol such that the stream register can receive streamed data items from the FIFO memory and supply them to the processor in the received order (column 1, lines 24 – 36).

34. As to claim 25, Baker teaches a system, further comprising a timeout generator, arranged for communication with the processor and the stream register, and arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, after a predetermined period of time, send a timeout signal to the processor,

causing the processor to interrupt such that it can execute other instructions (column, lines).

35. As to claim 26, Baker teaches a stream register, comprising:

a receiver arranged to receive a request for a data item from the processor (column 1, lines 24 – 36); and

a stream engine, arranged to send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item, and, if the data item is available, send the data item to the processor and if the data item is no available, send a timeout signal to the processor (column 12, lines 35 – 46).

36. As to claim 27, Baker teaches a stream register, wherein the stream engine is arranged to the interrupt signal to the processor after a predetermined period of time (column 24, lines 54 - 67).

37. As to claim 28, Baker teaches a stream register, wherein the stream engine is further arranged to, if the data is available, temporarily store the data in a register file for access by the processor (column 18, lines 13 – 67, column 19, lines 1 - 67).

38. As to claim 29, Baker teaches a stream register, wherein the stream engine is further arranged to, following sending of the timeout signal to the processor, if the data

item subsequently becomes available, receive a signal instructing it to cease sending the timeout signal, and to, upon receipt of the said instruction, cease sending the timeout signal to the processor and temporarily store the data in a register file for access by the processor (column 12, lines 37 –43).

39. As to claim 30, Baker teaches a stream register, comprising:

a receiver arranged to receive a request for a data item from the processor (column 1, lines 24 – 36); and

a stream engine arranged to send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and if the data item is available, send the data item to eh processor and if the data item is not available, send a stall signal to the processor (column 12, lines 35 –46).

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571)272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/21/2005
AH

TAMMARA PEYTON
PRIMARY EXAMINER